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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/707,149	11/24/2003	Taqi N. Buti		1148

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EXAMINER	
HASSAN, AURANGZEB	

ART UNIT	PAPER NUMBER
2182	

DATE MAILED: 06/29/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/707,149	BUTI ET AL.	
	Examiner	Art Unit	
	Aurangzeb Hassan	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/24/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. Claim 5 is objected to because of the following informalities: recites "instruction buffer of claim 1, a number" and is missing transitional language. Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1 – 30 are rejected under 35 U.S.C. 102(b) as being anticipated by Favor (US Patent Number 5,819,056).

4. As per claims 1 and 16, Favor teaches an instruction buffer comprising: a memory array (instruction cache, element 214, figure 2 and 4) partitioned into multiple identical memory sub-arrays (figure 5) arranged in sequential order from a first memory sub-array (corresponding to element 510 instructions, figure 5) to a last memory sub-array (corresponding to element 530 instructions, figure 5), each memory sub-array having multiple instruction entry positions (rows of figure 5) and adapted to store a different instruction of a set of concurrent instructions in a single instruction entry

position of any one of said memory sub-arrays (multiple instructions in each row of figure 5), said set of concurrent instructions arranged in sequential order from a first instruction to a last instruction (elements 510, 520, 530, figure 5).

5. As per claims 2 and 17, Favor teaches an instruction buffer wherein: each instruction of said set of concurrent instructions is stored in a different memory sub-array and the set of concurrent instructions may wrap from said last memory sub-array to said first memory sub-array (pointer wrapping around from element 514 to element 522 of figure 5).

6. As per claims 3 and 18, Favor teaches an instruction buffer wherein when said set of concurrent instruction wraps around, each instruction that is wrapped is written to an instruction entry position in a corresponding memory sub-array that is one instruction entry position higher (position of element 522 is entry position higher than element 514 of figure 5) in a memory sub-array corresponding to each instruction that is not wrapped except an instruction wrapped from the last instruction entry position of the last memory sub-array wraps to the first instruction entry position of the first memory sub-array (in the condition of the pointer of element 534 wrapping around to element 512 the entry position would be lower at 512 than 534).

7. As per claims 4, 5, 19 and 20, Favor teaches an instruction buffer wherein each memory sub-array comprises single write port and single read port memory cells (read

port and a write port, column 4, lines 49 – 59).

8. As per claims 6 and 21, Favor teaches an instruction buffer wherein: each instruction entry position is defined by a physical instruction entry position and a corresponding logical instruction entry position (instructions loaded into instruction cache via a predecoder 270 allowing for a logical entry position in the predecoder and a physical in the cache, column 4, lines 60 – 67, column 5, lines 1 – 11), each logical instruction entry position in a particular memory sub-array is a fixed number higher than an immediately previous logical instruction entry position in said particular memory sub-array (figure 7, predecoder); said physical instruction entry positions in each memory sub-array are one logical instruction entry position higher than corresponding physical entry positions of a immediately previous memory sub-array (first instruction element 710 and second instruction element 710 of figure 7), the first physical instruction entry position and first logical instruction entry position of a first memory sub-array being the same (opcode and memory location same, column 35, lines 1 – 11); and each said instruction of said set of concurrent instructions is stored in consecutive logical instruction entry positions of said memory array (located on subsequent pages, column 35, lines 12 – 37).

9. As per claims 7 and 22, Favor teaches an instruction buffer further including: a rotator multiplexer (byte rotator, elements 430, 432, 434, figure 4) adapted to receive said set of concurrent instructions and direct each instruction of said set of concurrent

instructions to an entry position (via instruction buffer, element 408, figure 4) in different consecutive memory sub-arrays (via elements 450, 452, 454, figure 4); an output multiplexer adapted to order a sequence of instructions read out of said memory array to match the order of instructions in said set of concurrent instructions (multiplexing by rotators, column 13, lines 12 – 19); a write address decoder adapted to determine a write address of a wordline (32- bit words, figure 7) of said memory array to which said first instruction of said set of instructions will be written; and a read address decoder adapted to determine a read address of a wordline (32-bit words, figure 7) of said memory array from which a first instruction of a group of instructions will be read from (read/write decoders, elements 410, 412, 414, 416, 418, figure 4, operating in decoding cycle, column 13, lines 36 – 53) .

10. As per claims 8, 9, 23 and 24, Favor teaches an instruction buffer wherein: a maximum number of instructions in said set of concurrent instructions is equal to N instructions (N instructions, figure 5); said rotator multiplexer comprises N, N:1 multiplexers, each multiplexer adapted to select one of said N instructions and couple the selected instruction to one of said memory sub-arrays (rotators based on N instructions, figure 4).

11. As per claims 10, 11, 25 and 26, Favor teaches an instruction buffer wherein: a number of said physical entry positions in each said memory sub-array is equal to Q; N is equal to 8 and Q is equal to 8; the first instruction in said set of concurrent instructions

has a physical instruction entry position defined by a 6-bit address, a first set of 3-bits of said 6-bit address defining a physical entry position in each memory sub-array and a second set of 3-bits of said 6-bit address defining a position of said sub-array in said memory array (figure 4a, address field shown by circuit diagram); and said write address decoder comprises: a write wordline decoder adapted to generate an 8-bit address of said first set of 3-bits and a 1-bit to the left shifted 8-bit address of said 8-bit address; seven 2:1 address multiplexers, an output of each address multiplexer coupled to a corresponding wordline select of seven sequential memory sub-arrays beginning with said first memory sub-array, a first input of each address multiplexer coupled to said 8-bit address, a second input of each address multiplexer coupled to said shifted 8-bit address and the select input of each address multiplexer coupled to a logic circuit (column 10, lines 11 – 25), said logic circuit coupled to said second set of 3-bits; and said 8-bit address coupled to a wordline select of said last memory sub-array (buffer in each group 0-7, column 10, lines 26 – 39).

12. As per claims 12, 13, 27 and 28, Favor teaches an instruction buffer wherein: M equals 5 and a maximum number of instructions to be read out of said memory array concurrently is M instructions; and said output multiplexer comprises M, N:1 multiplexers (multiplex access to plurality of outputs, column 5, lines 66 – 67, column 6, liens 1 – 11).

13. As per claims 14 and 29, Favor teaches an instruction buffer wherein: a

maximum number of instructions in said set of concurrent instructions is equal to N instructions; a number of said memory sub-arrays in said memory array is N; a number of said physical entry positions in each said memory sub-array is equal to Q; and Q may or may not be equal to N (figure 5, concurrent instructions along groups 0 – 3, sub-array of 64 rows) .

14. As per claims 15 and 30, Favor teaches an instruction buffer wherein each memory sub-array is selected from the group consisting of static random access memory arrays (SRAM, column 3, lines 64 – 67), dynamic random access memory arrays (DRAM, column 1, lines 13 – 15), latch arrays (column 5, lines 3 – 4), or a register array (1-D array, column 4, lines 4 – 6).

Conclusion

15. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. US Patent Number 6,243,287 teaches a sub-array memory system with multiplexing and rotators within the claimed invention.

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aurangzeb Hassan whose telephone number is (571)272-8625. The examiner can normally be reached on Monday - Friday 9 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Huynh can be reached on (571)272-4147. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

AH

KIM HUYNH
SUPERVISORY PATENT EXAMINER
6/27/06